REMARKS

Claims 1-20 were examined and reported in the Office Action. Claims 1-20 are rejected. Claims 1, 10 and 18 are amended. Claims 1-20 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 103(a)

It is asserted in the Office Action that claims 1-20 are rejected in the Office Action under 35 U.S.C. §103(a), as being unpatentable over U.S. Patent No. 6,181,151 B1, issued to Wasson ("Wasson"). Applicant respectfully disagrees.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)) Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." *"All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of " [a]n integrated circuit comprising: a test controller having an instruction register and a test access port finite state machine (TAP FSM), said test controller generates a first global control signal; at least one logic unit controller; a test bus directly coupled between the test controller and the at least one logic unit controller; at least one design-for-test-feature coupled to the at least one logic unit controller; and a logic unit coupled to the at least design-for-test-

temporarily attached to a "tester" through input/output channels of the integrated circuit. The distributed test control scheme reduces the number of global test control lines, relaxes routing constraints on the test control lines, and adds greater flexibility in the physical placement of the test controller and test control logic.

Wasson discloses an integrated circuit (IC) tester 10 that is temporarily attached to a device under test (DUT). It is clear that the tester of Wasson is not part of the DUT. While Figure 1 of Wasson shows tester 10 with a DUT 14 included, the tester is clearly separate from any DUT and only temporarily attaches to tester channels via input/output terminals. This can easily be seen by the language of the specification of Wasson. For example, column 3, lines 63-67 asserts that "tester 10 is adapted for testing DUT's of the type having in addition to a set of logic signal input and output terminals, a set of "scan" terminals enabling the tester to ascertain states of internal DUT nodes not otherwise accessible via normal DUT output terminals." Further, it would not be practical to manufacture a tester for testing a single DUT when the tester includes a host computer 16, a disk drive 22, a system disk drive 17 and a disk controller 18.

Moreover, the ordinary skilled person in the art would know that a computer, disk drive, system disk drive and disk controller cannot fit on an IC. Wasson simply does not disclose, teach or suggest an IC comprising test components where the test instructions are generated and executed directly on the IC to be tested. The IC tester of Wasson is clearly external to any IC (DUT) to be tested. Moreover, Wasson does not teach, disclose or suggest all the limitations contained in Applicant's amended claims 1, 10 and 18, as listed above.

Additionally, including testing components directly on an IC for performing test instructions directly on a single IC component would not be a simple design choice. It is clear that the components of Wasson's tester 10 cannot be embedded or included on an IC or DUT to perform test instructions directly on the IC or DUT.

Since Wasson does not disclose, teach or suggest all the limitations contained in Applicant's amended claims 1, 10 and 18, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claims 1, 10 and 18 are not obvious over Wasson since a *prima facie* case of obviousness

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely 1- 20, patentably defines the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

PETITION FOR EXTENSION OF TIME

Per 37 C.F.R. 1.136(a) and in connection with the Office Action mailed on, NOVEMBER 19, 2003, Applicant respectfully petitions Commissioner for a one (1) month extension of time, extending the period for response to FRIDAY, MARCH 19, 2004. Please charge the amount of $110.00 to cover the Petition filing fee for one month extension of time, large entity, to Deposit Account No. 02-2666. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN

Dated: February 25, 2004

By _____
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CERTIFICATE OF FACSIMILE

I hereby certify that this correspondence is being transmitted via facsimile on the date shown below to the United States Patent and Trademark Office.

Nadya Gordon

Nadya Gordon — February 25, 2004
Signature — Date